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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/320,421	05/26/99	FORBES	L 303.586US1

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MM91/0718

EXAMINER	
TRAN, A	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 07/18/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/320,421	FORBES ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2001* .

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6-11,13-18,20-24,26-38 and 40-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6-11,13-18,20-24,26-38 and 40-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Continued Prosecution Application

1. The request filed on 6/21/2001 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/320421 is acceptable and a CPA has been established. An action on the CPA follows.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the dual-gated transistor must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Specification

The specification is objected as being misdescriptive. Page 10, lines 16-30, describes the pair of transistors M3, M5, and M4, M6 of each inverter, B 1 and B2, comprises a dual-gated MOSFET. It is well known in the art that a dual-gated transistor is an AND function circuit. However, the pair of transistors M3, M5 and M4, M6 are the OR function circuit. Therefore, the pair of transistors M3, M5 and M4, M6 can not be replaced with a dual-gated transistor.

Claim Rejections - 35 USC ,§ 112

3. The following is a quotation of the second paragraph of 35 U. S. C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 2, 17, 18, 20-24 and 26-45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is indefinite as being unclear as to "one of the pair of transistor" in line 10 is the same as "one of the pair of transistor" in line 13.

Claims 2, is rejected as including the indefiniteness of claim 1.

Claims 17, 23, 29, 32, 33, 37, 40, 44 and 45 are misdescriptive and renders the claims indefinite as reciting the pair of transistors M3, M5 and M4, M6 is a dual-gated transistor. It is well known in the art that a dual-gated transistor is an AND function circuit. However, the pair of transistors M3, M5 and M4, M6 are the OR function circuit. Therefore, the pair of transistors M3, M5 and M4, M6 can not be replaced with a dual-gated transistor.

Claims 18, 20-22, 24 and 26-28, 30, 32, 34-36, 38 and 41-43 are rejected as including the indefiniteness of one of the claims above.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S. C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1, 2, 4, 6, 7, 10, 11, 13,14, 17, 18, 20, 23, 24, 29, 33-38, 44 and 45 are rejected under 35 U.S.C. 102(e) as being anticipated by Austin (U.S. Patent No. 5982690).

As to claim 1, Austin discloses in figure 1D a circuit comprising: a pair of cross-coupled inverters (153, 155 and 154, 156), wherein each inverter includes: a transistor of a first conductivity type (155, 156); a pair of transistors of a second conductivity type (153, 154) coupled at a drain region and coupled at a source region, and wherein the drain region for the

pair of transistors in each inverter is coupled to a drain region of the transistor of the first conductivity type in the same inverter, is coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and is coupled to a gate of one of the pair of transistors in the other inverter of the pair of cross-couple inverters; a pair of input transmission lines (outputs of circuit 103), wherein each one of the pair of input transmission lines is coupled to a gate of one of the pair of transistors in each inverter; and a pair of output transmission lines(lat, /lat), wherein each one of the pair of output transmission lines is coupled to the drain region of the pair of transistors and the drain region of the transistor of the first conductivity type in each inverter.

As to claim 2, figure 1D shows the transistor of a first conductivity type is a p-channel metal oxide semiconductor (PMOS) transistor, and the pair of transistors of a second conductivity type are n-channel metal oxide semiconductor (NMOS) transistors.

Claim 4 recites similar limitations of claims 1 and 2. Furthermore, figure 1D shows the inputs of the amplifier (105) are bit lines. Therefore, it is rejected for the same reasons.

As to claim 6, it is inherent for the bit line capacitances are removed from the pair of output transmission lines.

As to claim 7, it is inherent for each bit line is coupled to a number of memory cells in an array of memory cells (52 of figure 1B).

Claims 10, 11, 13, 14, 17, 18, 20, 23, 29, 33-38, 44 and 45 recite similar limitations of claims 4-6. Therefore, they are rejected for the same reasons. Further called for claim 29, it is inherent for the memory circuit comprising a processor (figure 4).

As to claim 24, figure 1D shows the memory circuit includes a folded bit line memory circuit.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 8, 9, 15, 16, 21, 22, 26, 27 and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Austin (USP 5982690).

As to claims 8, 15, 21, 26 and 30, Austin's figure 1D shows all elements of the claims except for the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts. However, the selection of the power supply to be less than 1.0 Volts is seen as an obvious design expedient dependent upon particular environment of use to ensure optimum performance.

As to claims 9, 16, 22, 27 and 31, Austin 's figure 1D shows all elements of the claims except for the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns). However, it is also seen as a design choice for designing the output speed of the sense amplifier to be able to output a full output sense voltage in less than 10 nanoseconds (ns) dependent upon particular environment of use to ensure optimum performance.

As to claim 32, Austin's figures 1D, 4 and 5 show all elements of the claim except for the processor and memory are formed on the same semiconductor substrate and integrated circuit. However, it is well known in the art that elements that from on the same semiconductor substrate and integrated circuit having the advantage of matching temperature and space and cost saving.

Therefore, it would have been obvious to one having ordinary skill in the art to make the processor and the memory to be formed on the same substrate and integrated circuit for the purpose of matching temperature and space or cost saving.

9. Claims 28 and 40-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko et al. (U.S. Patent No. 6069828) in view of Austin (U.S. Patent No. 5982690).

As to claims 28 and 40, Kaneko et al. teaches in figure 2 a memory circuit, and a method thereof, comprising a number of memory arrays (two sides of sense amplifier 15); a sense amplifier (15), a complementary pair of bit lines (BL1, BL1, BL2, BL2) input to the sense amplifier, a number of equilibration (14a, 14b), and a number of isolation transistorsm(18a, 18b). Thus, figure 2 shows all elements of the claim except for the detail of the sense amplifier. However, Austin shows in figure 1D a sense amplifier circuit comprising a pair of cross-coupled inverters (153, 155 and 154, 156), wherein each inverter includes: a PMOS transistor (155, 156), a dual-gated NMOS transistor (153, 154) wherein the drain region for the dual-gated NMOS transistor is coupled to a drain region of the PMOS transistor; a pair of bit lines (outputs of 103), wherein each one of the pair of bit lines is coupled to a first gate of the dual-gated transistor in each inverter; and a pair of output transmission lines (out, /out), wherein each one of the pair of output transmission lines is coupled to the drain region of the dual-gated NMOS transistor and the drain region of the PMOS transistor in each inverter. Austin's amplifier circuit having the advantage of reducing power dissipation. Therefore, it would have been obvious to one having an ordinary skill in the art to use the Austin's sense amplifier circuit for Kaneko et al.'s figure 2 for the purpose of reducind power dissipation.

As to claim 40, Austin's figure 1D shows all elements of the claims except for the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts. However, the selection of the power supply to be less than 1.0 Volts is seen as an obvious design expedient dependent upon particular environment of use to ensure optimum performance.

As to claim 41, Austin 's figure 1D shows all elements of the claims except for the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns). However, it is also seen as a design choice for designing the output speed of the sense amplifier to be able to output a full output sense voltage in less than 10 nanoseconds (ns) dependent upon particular environment of use to ensure optimum performance.

As to claim 43, from the rejection above, it is inherent for the sense amplifier removes the bit line capacitance from a pair of output nodes of the sense amplifier.

Response to Arguments

9. Applicant's arguments have been fully considered but they are not persuasive.

In the drawing: Applicant states the dual-gated transistors, as defined page 10, line 16-20 of the Applicant's specification, is comprised of the combination of M4 and M6 having a shared body region. However, line 16-20 of the Applicant's specification does not teach the dual gate transistor is two parallel transistors having a shared body region. Furthermore, the drawing is not clearly shown M3 and M5, or M4 and M6, having a shared body region. Therefore, the dual-gated transistor can not be interpreted as a combination of two parallel transistors having a share body region. It is well known in the art that dual-gated transistor is a two series connected transistors having a shared body region. The 6104068 reference is patented after the present invention. Therefore, the dual gated transistor which is the combination of two parallel

transistors having a shared body region was not well known in the art at the time of the invention.

Similar reasons in response to the arguments of the specification objection and the 35 U.S.C. 112 rejection of the claims in the previous office action.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is (703) 308-6174. The examiner can normally be reached on Monday to Friday from 7:40 am to 4:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reach at (703) 308-4876. The fax phone number for this group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

QT

QT

July 2, 2001

Terry D. Cunningham
Primary Examiner